Charge Module E Datasheet

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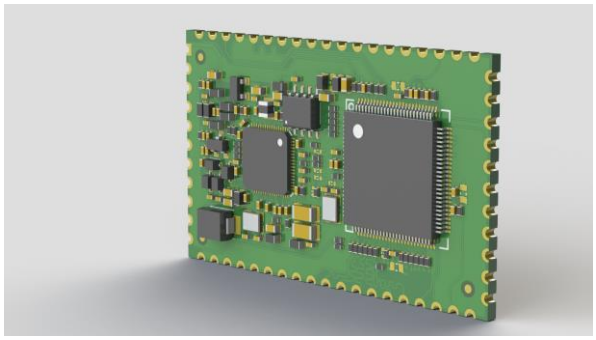
Contents

Introduction

Charge Module E adds DIN 70121 and ISO 15118 functionality to the EVSE side. It provides all core functionalities to enable chargers the high level communication with a CCS enabled EV.

The Module is equipped with a QCA7005 and a powerful Cortex M4 running a state-of-the-art Real time Operating System with our complete SW stack included. It will provide your charger with all the necessary parameters from the EV.



Key Features

- Dual mode ISO 15118/DIN 70121 SW Stack
- IEC 61851 and ISO 15118
- Ready for Plug and Charge
- Ready for Bidirectional charging
- TLS 1.3
- CAN-interface
- UART-interface
- Multiple modules on same CAN interface
- Automotive ready
- UDS support for diagnostics and configuration

Operational

Parameter	Value
Weight	< 10 g
Temperature range	-40 °C - 85 °C
RoHS / reach	This product is manufactured RoHS / reach compliant.
Power supply	3.3 V
Power consumption	max. 350 mA
Outline dimension	50.8 mm x 30.48 mm

Applications

- Generic charge communication controller for charging stations or wall boxes

Interfaces

Charge Module E has a CAN and UART interfaces for the customer application.

- CAN bus
  CAN is implemented in Charge Module E with baud rate running at default 500 Kbit/s. Messages are supporting extended IDs. A DBC-File is available on request.
- UART interface
  UART interface is implemented in Charge Module E with the below parameters' setup.

Parameter	Value
Baudrate	115200 bit/s
Start Bit	1
Stop Bit	1
Data Bits	8
Parity Bit	None
Flow Control	No

1 Module Overview

The block diagram in Figure 1 shows the module components in the gray box as well as the connections and external components that you need additionally.

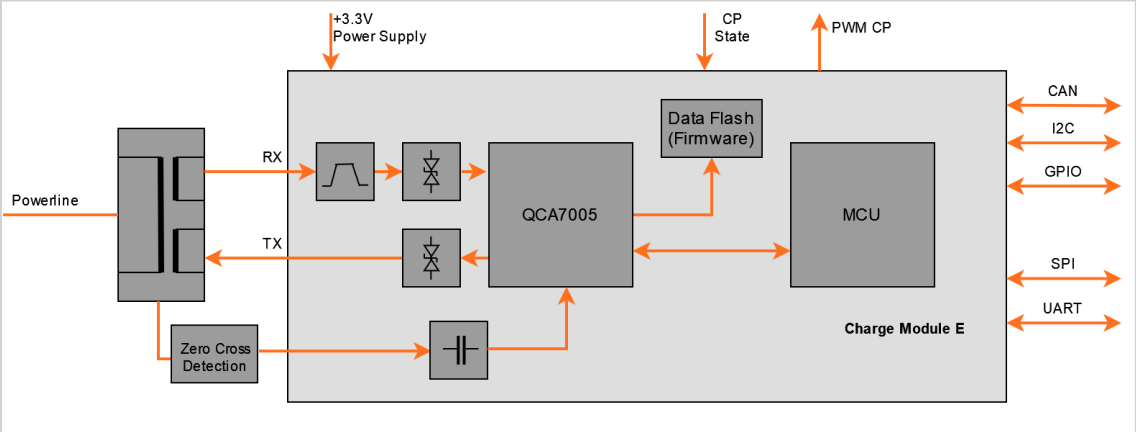


Figure 1 Block diagram

2 Electrical Characteristics

2.1 Absolute maximum ratings

Symbol	Maximum parameter	Min	Max	Unit
V_{DD}	Digital supply voltage	-0.3	3.46	V
V_{DIO}	Digital input voltage	-0.3	3.6	V
T_{STORE}	Storage temperature	-40	+85	°C
R_{AH}	Relative air humidity (not condensing)	10	90	%

Table 1 Absolute Maximum Ratings

2.2 Recommended operating conditions

2.2.1 Supply parameter

Symbol	Supply Parameter	Min	Typ	Max	Unit
V_{DD}	DC supply voltage	3.13	3.3	3.46	V
I_{DD}	Current for VDD	-	-	350	mA
I_{GPIO}	GPIO current	-	3.5	14	mA

Table 2 Supply Parameter

2.2.2 GreenPHY powerline communication parameter

PLC on Control pilot parameter	Min	Typ	Max	Unit
Reach	-	-	300	m
Data rate	-	-	10	Mbit/s

Table 3 GreenPHY Powerline Communication Parameter

2.2.3 Digital input parameter

Digital input parameter	Min	Typ	Max	Unit
Input voltage	-	-	3.6	V

Table 4 Digital Input Parameter

2.2.4 Digital output parameter

Digital output parameter	Min	Typ	Max	Unit
Output voltage	-	2.5	3.3	V
Output current	-	3.5	14	mA

Table 5 Digital Output Parameter

3 Module Pinout

Pin	Name	Direction	Description
1	V_{DD}	SUPPLY	Supply Voltage for the Module
2	GND	SUPPLY	Ground connection
3	RXIN_N	IN	Powerline receiver input negative
4	RXIN_P	IN	Powerline receiver input positive
5	TXOUT_N	OUT	Powerline transmitter output negative
6	TXOUT_P	OUT	Powerline transmitter output positive
7	DIR[1]	IN	Reserved, connect to GND
8	GND	SUPPLY	Ground connection
9	GND	SUPPLY	Ground connection
10	GND	SUPPLY	Ground connection
11	RSVD_01		Reserved
12	RSVD_02		Reserved
13	RSVD_03		Reserved
14	RSVD_04		Reserved
15	RSVD_05		Reserved
16	HW_Strap_1	IN	Interface selection. UART: 3.3 kOhms PullUp CAN: 3.3 kOhms PullDown
17	RSVD_06		Reserved
18	RSVD_07		Reserved
19	RSVD_08		Reserved
20	UART_TX	OUT	UART TX
21	UART_RX	IN	UART RX
22	RSVD_09		Reserved
23	RSVD_10		Reserved
24	RSVD_11		Reserved
25	RSVD_12		Reserved
26	RSVD_13		Reserved
27	CAN_RX	IN	CAN RX channel
28	CAN_TX	OUT	CAN TX channel
29	PP_value[2]	ADC	Proximity pilot ADC signal, RC low pass filter present on PCB (f_c = 160 kHz)
30	SPI_CLK	IN	SPI Clock (master→slave)
31	SPI_DI	IN	SPI data MOSI (master→slave)
32	SPI_DO	OUT	SPI data MISO (slave→master)
33	SPI_CS_L	IN	SPI Chip select (master→slave), low active
34	IRQ_O	OUT	SPI interrupt (slave→master)
35	I2C_SCL	OUT	Reserved
36	I2C_SDA	IN/OUT	Reserved
37	EV_CP_Edge	IN	Reserved for Charge Module S
38	CP_State_C	OUT	Reserved for Charge Module S
39	RSVD_14[2]	ADC	Reserved
40	CP_RST_Neg	OUT	CP State, reset negative peak voltage detection
41	CP_RST_Pos	OUT	CP State, reset positive peak voltage detection
42	CP_PWM_out	OUT	CP PWM generation
43	CP_Pos_Peak_det[2]	ADC	CP State, positive peak voltage detection, ADC signal, RC low pass filter present on PCB (f_c = 160 kHz)

Pin	Name	Direction	Description
44	CP_Neg_Peak_det[2]	ADC	CP State, negative peak voltage detection ADC signal, RC low pass filter present on PCB (f_c = 160 kHz)
45	CP_PWM_INV	OUT	CP PWM enable (low active)
46	GPIO_2	IN/OUT	Customer GPIO
47	GPIO_3	IN/OUT	Customer GPIO
48	GPIO_4	IN/OUT	Customer GPIO
49	GPIO_5	IN/OUT	Customer GPIO
50	BL_BD[3]	IN	Bootloader backdoor input Bootloader state: 3.3 kOhms PullUp Application state: 3.3 kOhms PullDown
51	Trace_CLK_OUT	OUT	Trace clock out
52	Trace_D3	OUT	Trace data out 3
53	Trace_D2	OUT	Trace data out 2
54	Trace_D1	OUT	Trace data out 1
55	Trace_D0	OUT	Trace data out 0
56	JTAG_TDO	OUT	Test data output
57	JTAG_TDI	IN	Test data input
58	JTAG_TCLK	IN	Test clock
59	RESET_L[4]	IN	Reset input pin, low active
60	JTAG_TMS	IN/OUT	Test mode selection

Table 6 Module Pinout

[1] Connect directly to GND for normal operation.

[2] If ADC is not used, connect to GND with 10 kOhms series resistor.

[3] Connect this pin to 3.3V if the module shall be forced to stay in the bootloader. Otherwise connect to GND. This pin is connected to an internal pull down resistor.

[4] The RESET pin is driven low by the MCU for at least 128 bus clock cycles and until flash memory initialization has completed.

[5] Unused digital pins can be left floating. It is recommended to connect the unused pins to GND with 10 kOhms series resistor.

4 Module Dimensions

Figure 2 shows the physical dimensions of the module. Pin 1 is a rectangular shaped pad on the top side of the module.

All dimensions are in mm, the pads are all of the same size and distances between pads are equal if not otherwise specified in the drawing.
Bow & twist is max. 0.5% for the module.

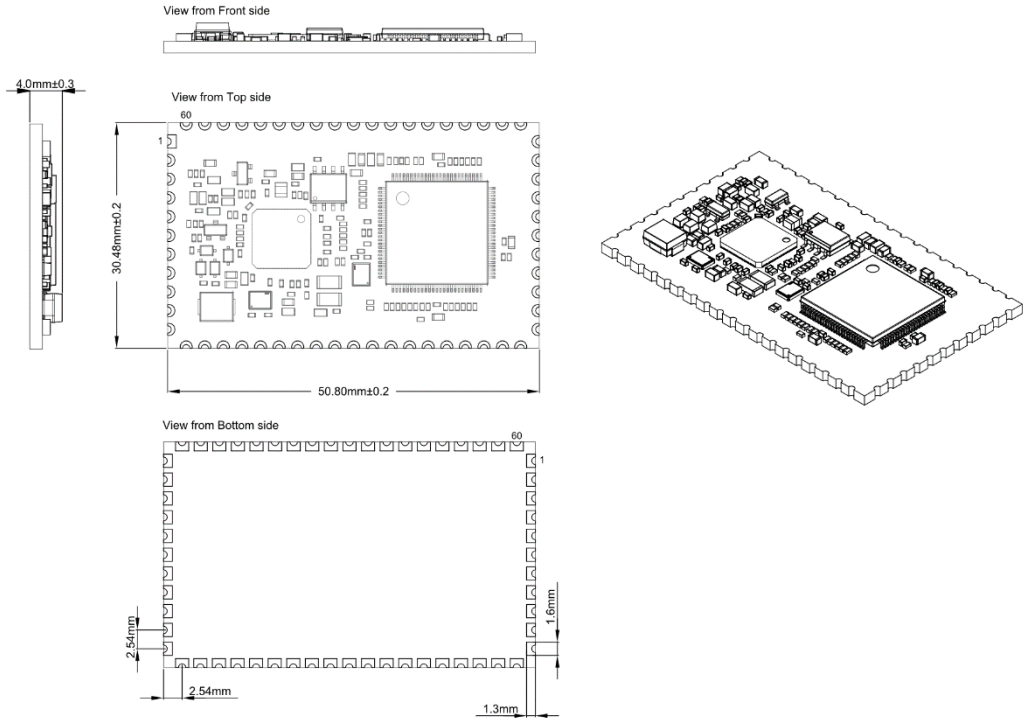


Figure 2 Charge Module E dimensions

5 Footprint Dimensions

Figure 3 shows the recommended footprint for the Charge Module E. The module outline shows the ideal measures, tolerance is not included.

The area between the pads should kept free of copper on the base PCB.

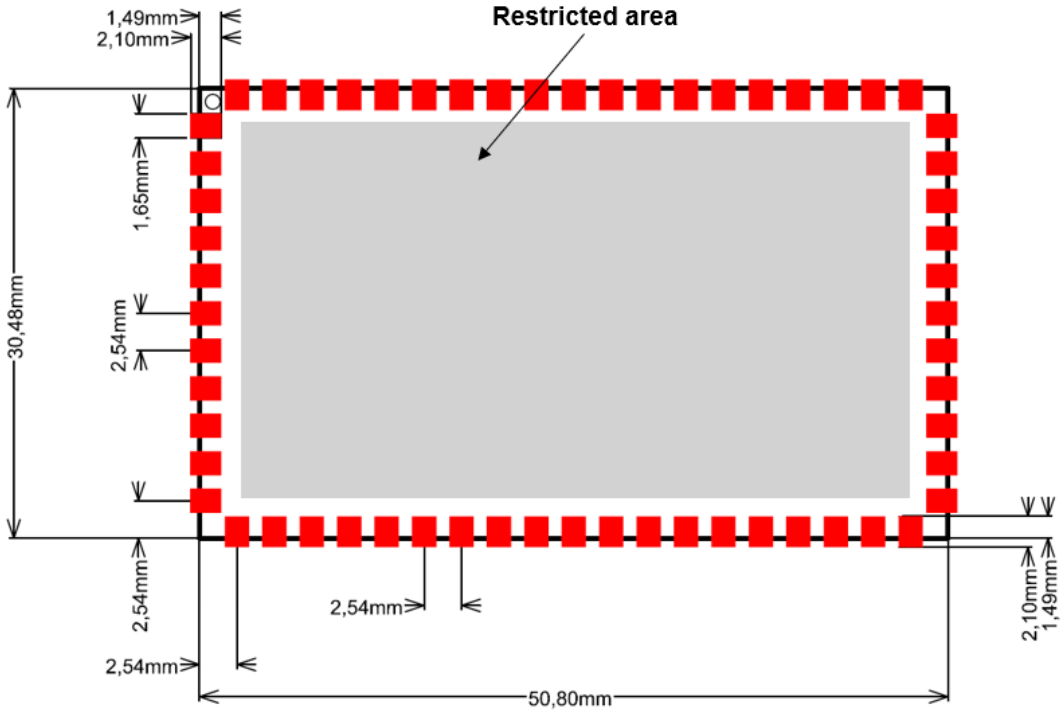


Figure 3 Charge Module E footprint

6 Reference Schematics

A possible implementation of the coupling circuit is shown in Figure 4 for coupling to automotive applications. This schematic is freely based on the QCA7000 / QCA7005 Add-In reference schematic by Qualcomm Atheros.

chargebyte GmbH provides you with all non-standard parts you will need to implement this design into your own application.

Version	Order Code
1:1:1 for Electric Vehicle (PEV) and Electric Vehicle Supply Equipment (EVSE)	I2PLCTR-5

Table 7 Available Accessories

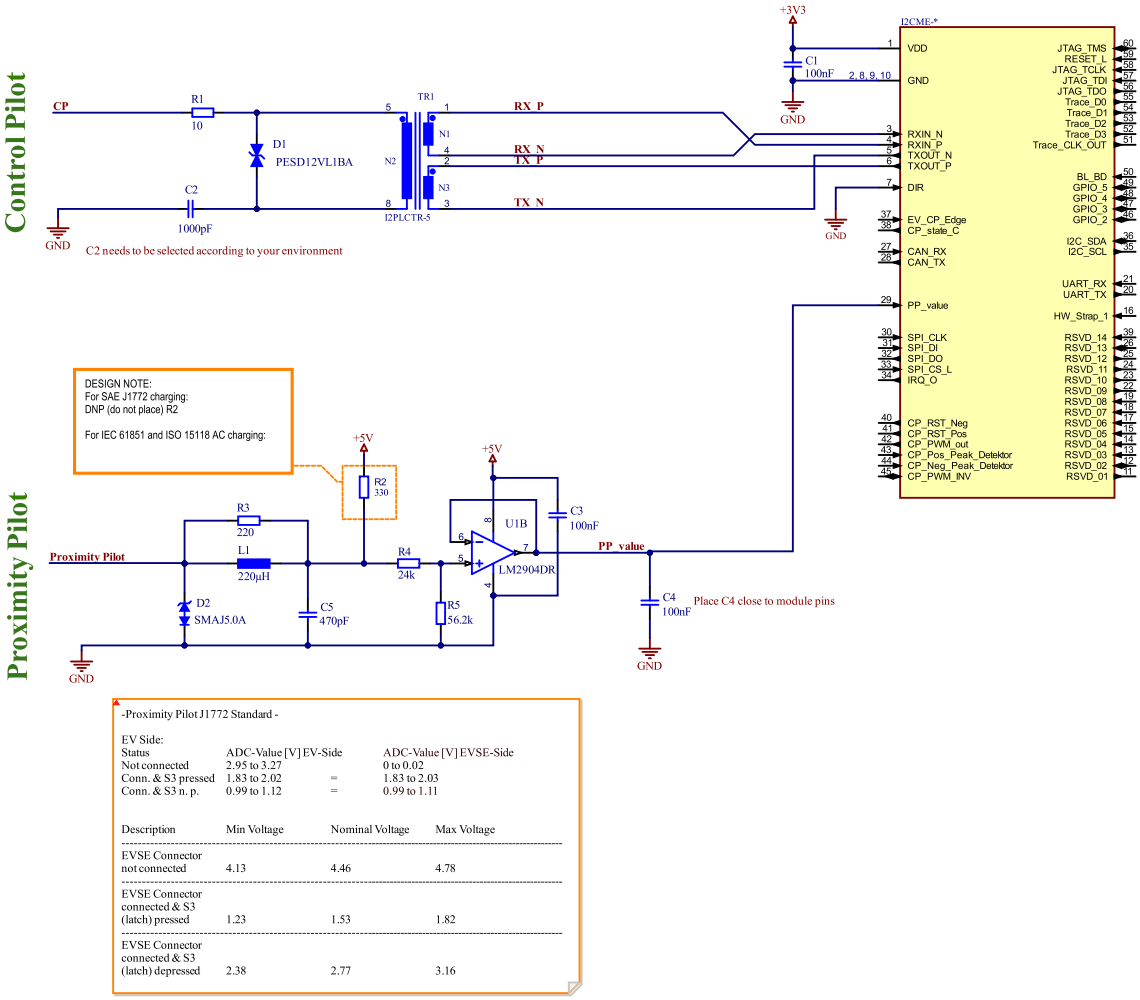


Figure 4 EVSE CP, PP reference schematic

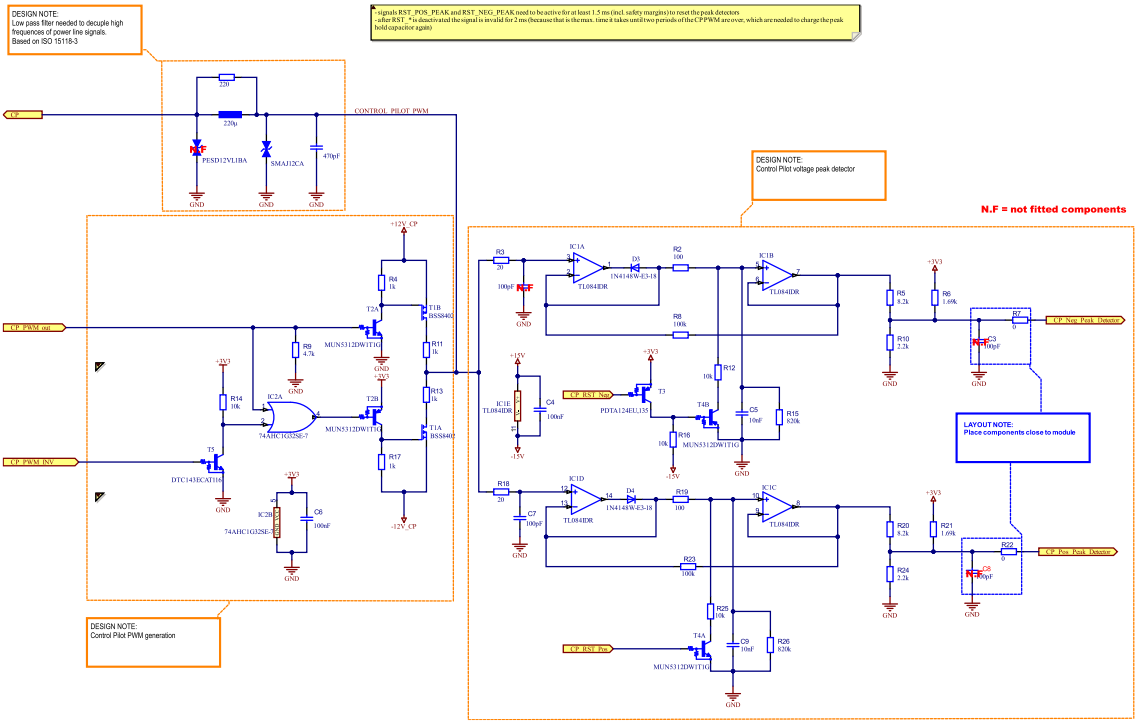


Figure 5 EVSE CP generation and voltage read reference schematic

7 Cryptochip for TLS encryption

To enable a TLS functionality in future firmware releases, the cryptochip SE050C1HQ1/Z01SCZ from NXP has to be connected to the I2C interface of the module.
The TLS encryption is a mandatory requirement for the ISO15118-20 protocol and optional for ISO15118-2. This cryptochip is mandatory to comply with this requirement with the Charge Module E firmware.
A reference schematic can be found in NXP's technical documentation of the cryptochip.

8 Module Marking

Each Module is marked with a label containing the following data:

- Data Matrix Code with following Information (space separated Values):
  - Order Code
  - MAC Address QCA7005
  - MAC Address Host
  - Serial Number

9 Packaging Information

9.1 Tray

CME standard packing 25 modules per tray. Trays shall be used in a rolling system.

Figure 6 Packing example

9.2 Reel

The CME tape & reel packing contains 200 modules per reel.
Modules from cut tape & reel in less quantity than 200 pcs can be provided by request. In that case modules will be provided with a tape & reel section only missing the core.

Material: Polystyrene

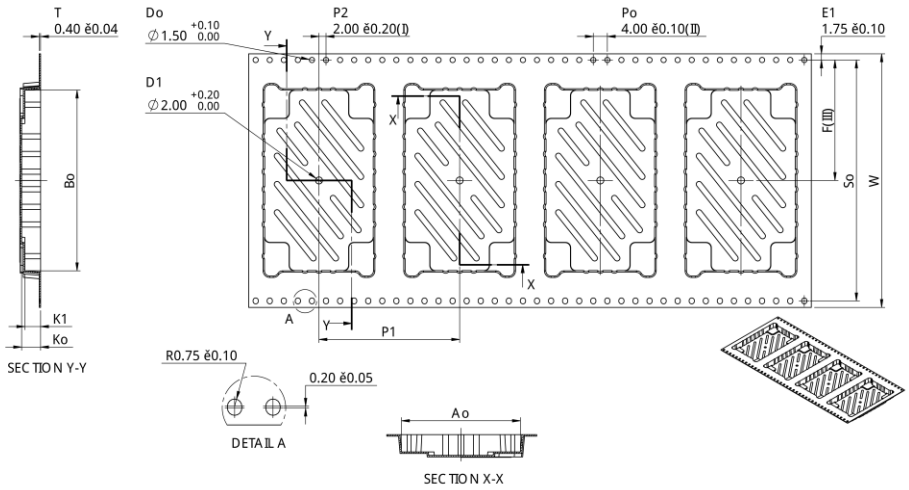


Figure 7 Tape and Reel Technical Drawing

Ao	31.00	+/- 0.15
Bo	51.30	+/- 0.15
Ko	5.40	+/- 0.15
K1	4.50	+/- 0.15
F	34.20	+/- 0.30
P1	40.00	+/- 0.15
So	68.40	+/- 0.20
W	72.00	+/- 0.30

Table 8 Tape and Reel Technical Drawing Dimensions

All dimensions in millimeters unless otherwise stated.

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is +/- 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension with () is used for design reference purpose.
No measurement required.

10 Order Code Compilation

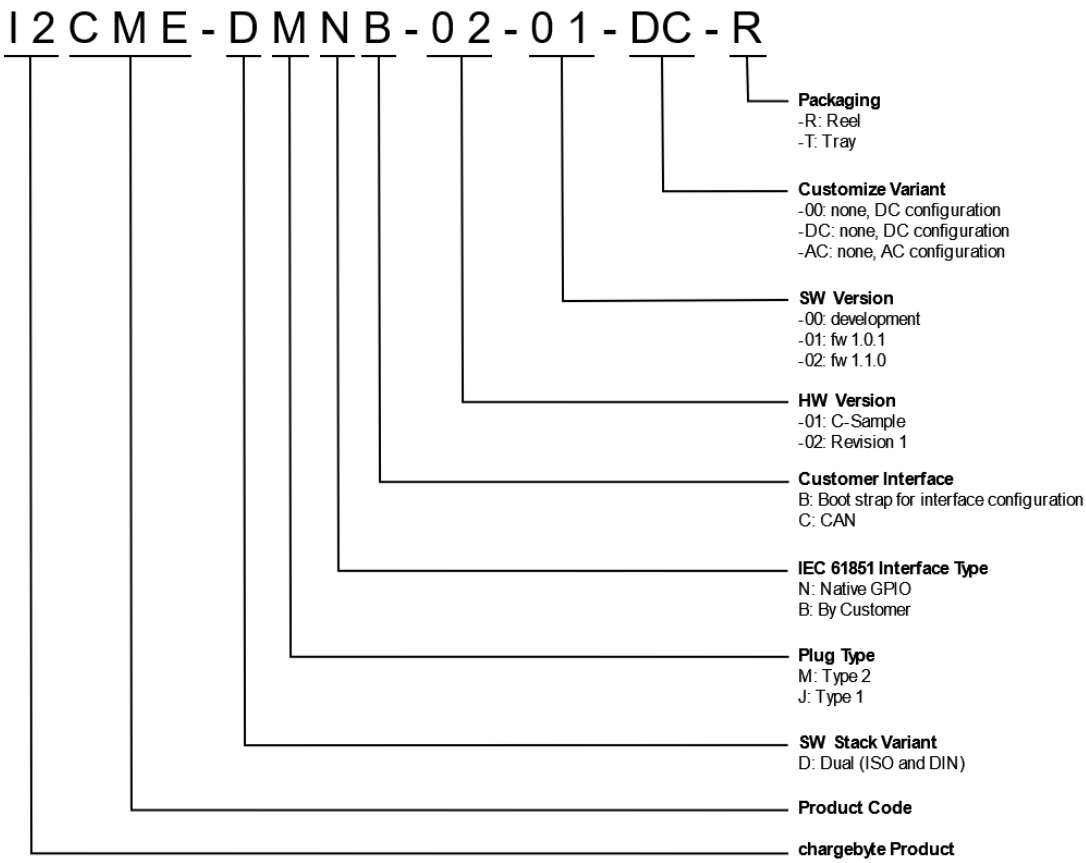


Figure 8 Order Code Compilation

11 Order Information

The following table provides an overview of the available Charge Module E variants

Order Code	Plug Type	IEC 61851 Interface	HW Version	SW Version	Customize Variant
I2CME-DMNB-02-01-DC-R/T	Type 2	Native GPIO	Revision 1	1.0.1	none, DC
I2CME-DMNB-02-02-DC-R/T	Type 2	Native GPIO	Revision 1	1.1.0	none, DC
I2CME-DMBB-02-02-DC-R/T	Type 2	By Customer	Revision 1	1.1.0	none, DC

Table 9 Charge Module E Order Codes

12 Handling

This electronic component is sensitive to **electrostatic discharge (ESD)**.

- Process the modules according to IPC/JEDEC J–STD-020 and J-STD-033 guidelines.
- Limit repeated reflow processes to maximum 2.

The module contains components with **moisture sensitivity level (MSL) 3**. Please handle them accordingly.

13 Revisions

Revision	Release Date	Changes
9	21 February 2024	Added information for bow & twist percentage Added I2PLCTR-5 to reference schematics and BOM Updated Order Information Updated Order Code Compilation with firmware 1.0.1 and 1.1.0 Updated section “Reel”
8	10 July 2023	Updated table Module Pinout (renamed PIN7) Updated PIN39 with internal pulldown Updated figure EVSE CP generation and voltage read reference schematic Added "Packaging Information"
7	17 May 2023	Updated Module Pinout (renamed PIN39 to RSVD_14) Updated figure for EVSE CP, PP, ZC reference schematic Updated table Module Pinout Added "Cryptochip for TLS encryption"
6	19 September 2022	Add Module Dimensions Added UART Pins Updated figure "Module Dimensions" Updated company contact Updated the key features and module interfaces
5	16 November 2021	Updated Figure 4 (EVSE CP generation and voltage read reference schematic) Updated table Module Pinout Updated table Supply parameter (changed min. DC supply voltage to 3.13V)
4	19 October 2021	Corporate Identity Beautified Figures
3	18 October 2021	Updated CP generation reference schematic
2	17 June 2021	Added Schematics UDS protocol feature Added Zero cross detection Added Pin 1 marking at mechanical dimensions Updated Module marking
1	18 May 2021	Initial release

14 Contact

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