Charge Module E Datasheet

chargebyte GmbH

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Charge Module E adds DIN 70121 and ISO 15118 functionality to the EVSE side. It provides all core functionalities to enable DC Chargers the high-level communication with a CCS enabled EV.

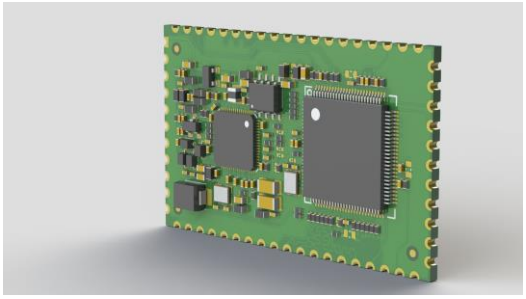
The Module is equipped with a QCA7005 and a powerful Cortex M4 running a state-of-the-art Real time Operating System with our complete SW stack included. It will provide your DC Charger with all the necessary parameters from the EV.

Key Features

- Dual mode ISO 15118/DIN 70121 SW Stack
- IEC 61851 and ISO 15118
- Ready for Plug and Charge
- Ready for Bidirectional charging
- TLS 1.3
- CAN-interface
- UART-interface
- Multiple modules on same CAN interface
- Automotive ready
- UDS support for diagnostics and configuration

Operational

Parameter	Value
Weight	< 10 g
Temperature range	-40 °C - 85 °C
RoHS / reach	This product is manufactured RoHS / reach compliant.
Power supply	3.3 V
Power consumption	Max. 350 mA
Outline dimension	50.8 mm x 30.48 mm



Applications

- Generic charge communication controller for DC Charge Stations or DC Wall boxes

Interfaces

Charge Module E has a CAN and UART interfaces for the customer application.

- CAN bus
  CAN is implemented in Charge Module E with baud rate running at default 500 Kbit/s. Messages are supporting extended IDs. A DBC-File is available on request.
- UART interface
  UART interface is implemented in Charge Module E with the below parameters' setup.

Parameter	Value
Baudrate	115200 bit/s
Start Bit	1
Stop Bit	1
Data Bits	8
Parity Bit	None
Flow Control	No

Contents

1 Module Overview

The block diagram in Figure 1 shows the module components in the gray box as well as the connections and external components that you need additionally.

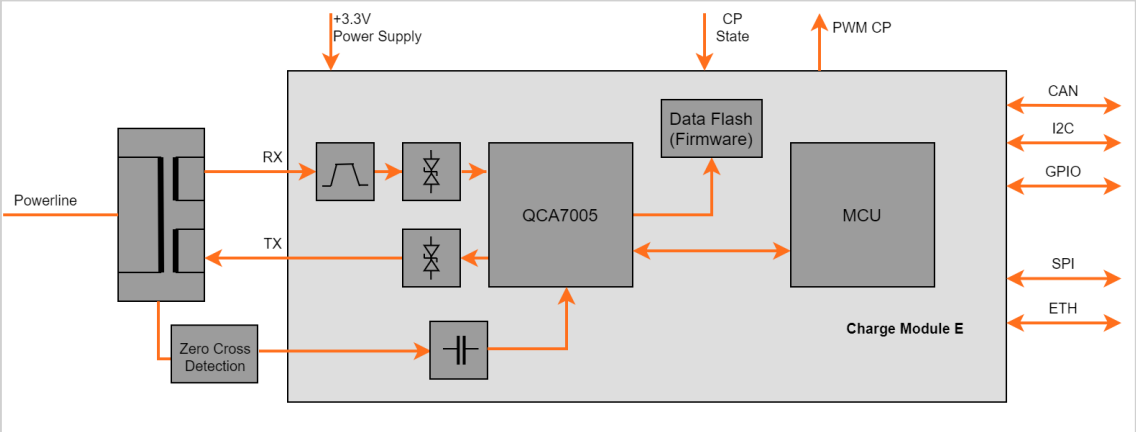


Figure 1 Block diagram

2 Electrical Characteristics

2.1 Absolute maximum ratings

Symbol	Maximum parameter	Min	Max	Unit
V_{DD}	Digital supply voltage	-0.3	3.46	V
V_{DIO}	Digital input voltage	-0.3	3.6	V
V_{PP}	Proximity pilot voltage	-0.3	3.3	V
T_{STORE}	Storage temperature	-	-	°C
R_{AH}	Relative air humidity (not condensing)	10	90	%

2.2 Recommended operating conditions

2.2.1 Supply parameter

Symbol	Supply Parameter	Min	Typ	Max	Unit
V_{DD}	DC supply voltage	3.13	3.3	3.46	V
I_{DD}	Current for VDD	-	-	350	mA
I_{GPIO}	GPIO current	-	3.5	14	mA

2.2.2 GreenPHY powerline communication parameter

PLC on Control pilot parameter	Min	Typ	Max	Unit
Reach	-	-	300	m
Data rate	-	-	10	Mbit/s

2.2.3 Digital input parameter

Digital input parameter	Min	Typ	Max	Unit
Input voltage	-	-	3.6	V

2.2.4 Digital output parameter

Digital output parameter	Min	Typ	Max	Unit
Output voltage	-	2.5	3.3	V
Output current	-	3.5	14	mA

3 Module Pinout

Pin	Name	Direction	Description
1	V_{DD}	SUPPLY	Supply Voltage for the Module
2	GND	SUPPLY	Ground connection
3	RXIN_N	IN	Powerline receiver input negative
4	RXIN_P	IN	Powerline receiver input positive
5	TXOUT_N	OUT	Powerline transmitter output negative
6	TXOUT_P	OUT	Powerline transmitter output positive
7	ZC_IN	IN	Zero cross detection input
8	GND	SUPPLY	Ground connection
9	GND	SUPPLY	Ground connection
10	GND	SUPPLY	Ground connection
11	MII_RMII_MDC	OUT	Reserved
12	MII_RMII_MDIO	IN_OUT	Reserved
13	MII_RX_CLK	IN	Reserved
14	MII_RMII_RXD0	IN	Reserved
15	MII_RMII_RXD1	IN	Reserved
16	MII_RXD2	IN	Reserved
17	MII_RXD3	IN	Reserved
18	MII_RMII_RX_DV	IN	Reserved
19	MII_RMII_RX_ER	IN	Reserved
20	UART_TX	OUT	UART TX
21	UART_RX	IN	UART RX
22	MII_RMII_TXD1	OUT	Reserved
23	MII_TXD2	OUT	Reserved
24	MII_TXD3	OUT	Reserved
25	MII_RMII_TX_EN	OUT	Reserved
26	MII_RMII_TX_CLK	OUT	Reserved
27	CAN_RX	IN	CAN RX channel
28	CAN_TX	OUT	CAN TX channel
29	PP_value	IN	Proximity pilot ADC signal
30	SPI_CLK	IN	SPI Clock (master→slave)
31	SPI_DI	IN	SPI data MOSI (master→slave)
32	SPI_DO	OUT	SPI data MISO (slave→master)
33	SPI_CS_L	IN	SPI Chip select (master→slave), low active
34	IRQ_O	OUT	SPI interrupt (slave→master)
35	I2C_SCL	OUT	Reserved
36	I2C_SDA	OUT	Reserved
37	EV_CP_Edge	IN	Reserved for Charge Module S
38	CP_State_C	OUT	Reserved for Charge Module S
39	EV_CP_Bufferd	IN	Reserved
40	CP_RST_Neg	OUT	CP State, reset negative peak voltage detection
41	CP_RST_Pos	OUT	CP State, reset positive peak voltage detection
42	CP_PWM_out	OUT	CP PWM generation
43	CP_Pos_Peak_det	IN	CP State, positive peak voltage detection, ADC signal
44	CP_Neg_Peak_det	IN	CP State, negative peak voltage detection ADC signal
45	CP_PWM_INV	OUT	CP PWM enable (low active)
46	GPIO_2	IN/OUT	Reserved GPIO
47	GPIO_3	IN/OUT	Reserved GPIO
48	GPIO_4	IN/OUT	Reserved GPIO
49	GPIO_5	IN/OUT	Reserved GPIO

Pin	Name	Direction	Description
50	GPIO_6	IN/OUT	Reserved GPIO
51	Trace_CLK_OUT	OUT	Trace clock out
52	Trace_D3	OUT	Trace data out 3
53	Trace_D2	OUT	Trace data out 2
54	Trace_D1	OUT	Trace data out 1
55	Trace_D0	OUT	Trace data out 0
56	JTAG_TDO	OUT	Test data output
57	JTAG_TDI	IN	Test data input
58	JTAG_TCLK	IN	Test clock
59	RESET_L	IN	Reset input pin, low active
60	JTAG_TMS	IN/OUT	Test mode selection

Table 1 Module Pinout

*The RESET pin is driven low by the MCU for at least 128 bus clock cycles and until flash memory initialization has completed.

4 Module Dimensions

Figure 2 shows the physical dimensions of the module. Pin 1 is a rectangular shaped pad on the top side of the Module.

All dimensions are in mm, the pads are all of the same size and distances between pads are equal if not otherwise specified in the drawing.

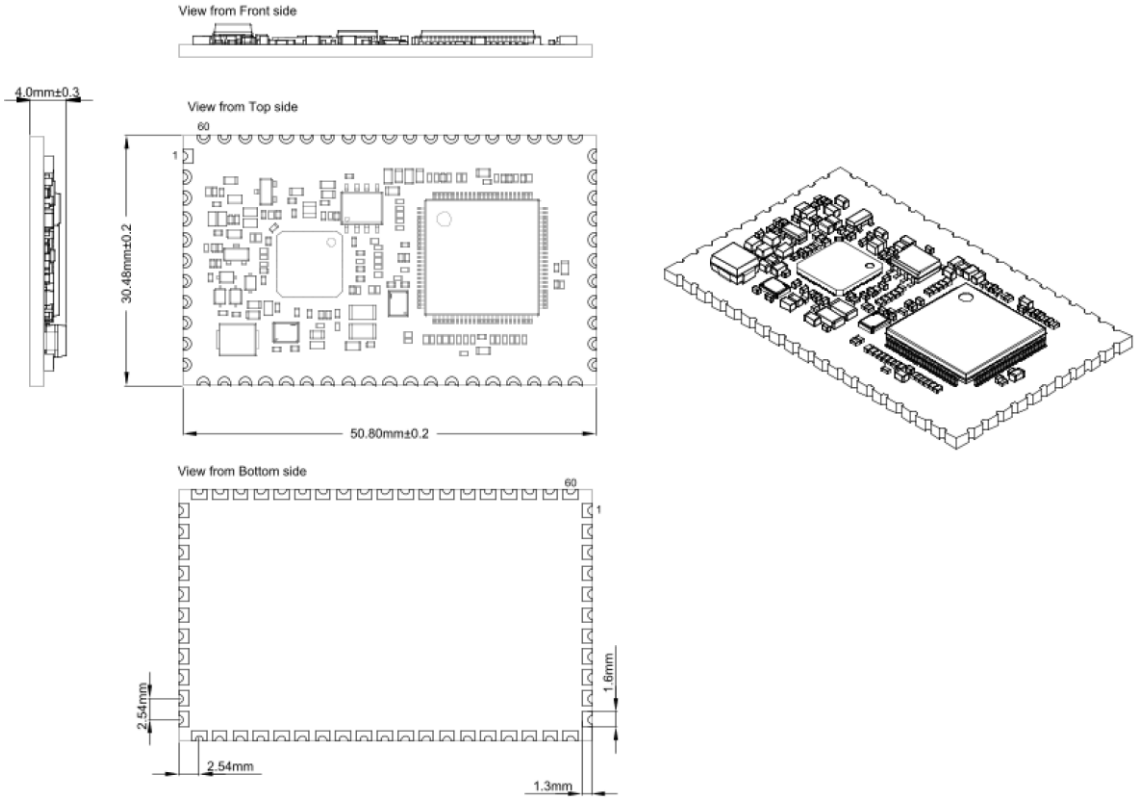


Figure 2 Charge Module E dimensions

5 Footprint Dimensions

Figure 3 shows the recommended footprint for the Charge Module E. The module outline shows the ideal measures, tolerance is not included.

The area between the pads should kept free of copper on the base PCB.

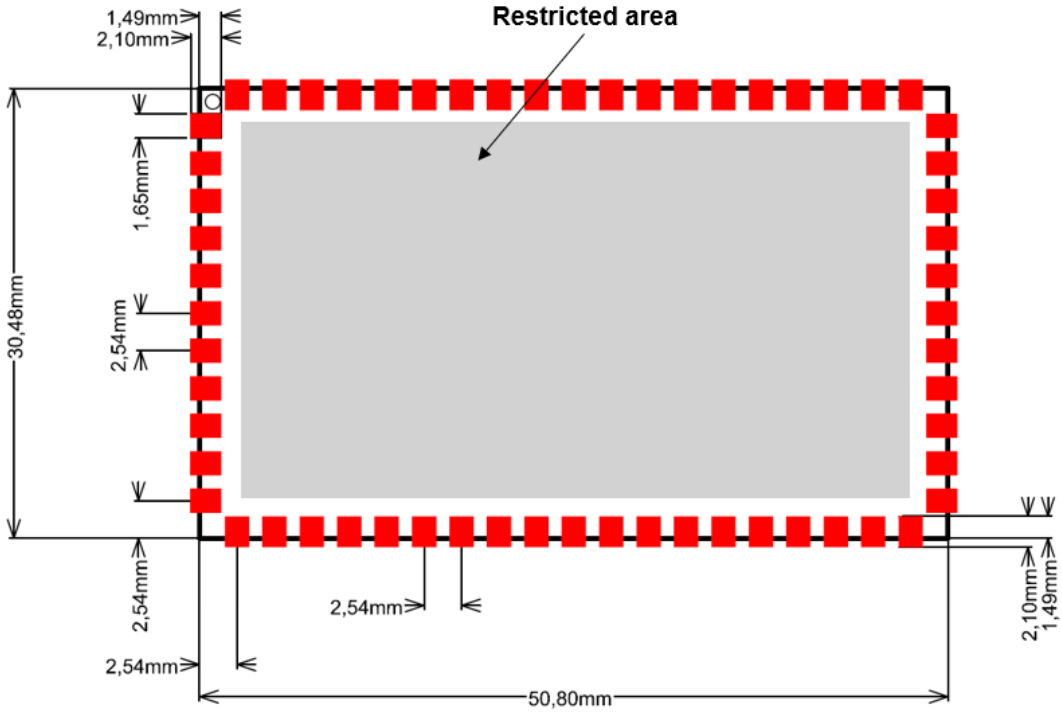


Figure 3 Charge Module E footprint

6 Reference Schematics

A possible implementation of the coupling circuit is shown in Figure 4 for coupling to automotive applications. These schematic is freely based on the QCA7000 / QCA7005 Add-In reference schematic by Qualcomm Atheros. If you are not sure if the signals will couple to other lines where PLC communication is used, you should connect the zero cross detector to your mains port. For use together with electric vehicles (PEV) the signal ZC IN needs to be connected to GND.

chargebyte GmbH provides you with all non-standard parts you will need to implement this design into your own application.

The PP reference schematic is currently under revision and will be available in the next version of this document.

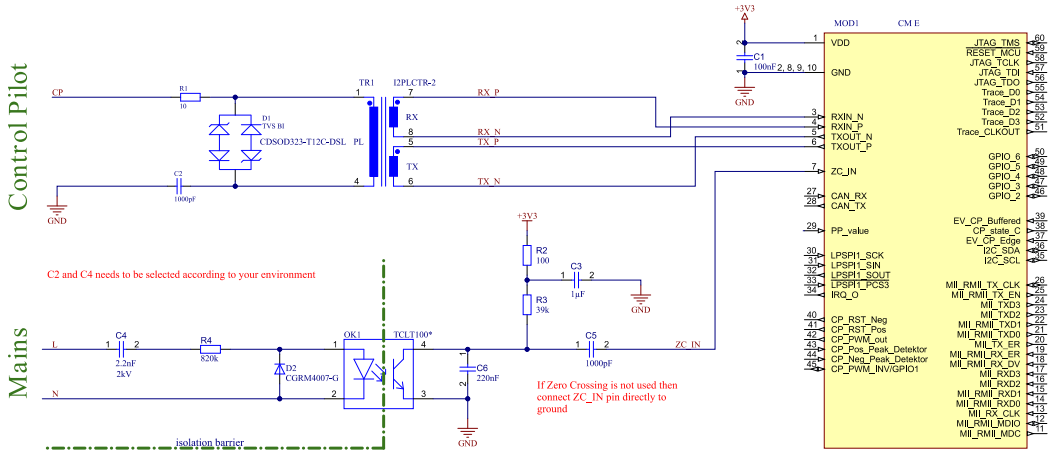


Figure 4 EVSE CP, PP, ZC reference schematic

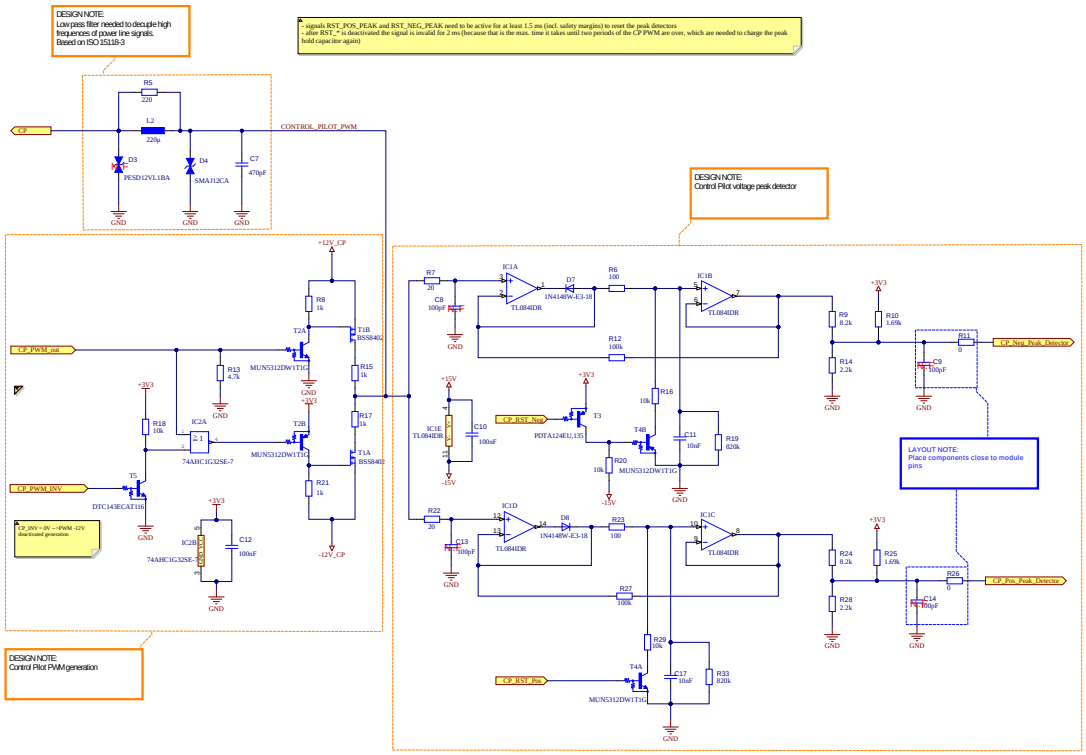


Figure 5 EVSE CP generation and voltage read reference schematic

7 Module Marking

Each Module is marked with a label containing the following data:

- Data Matrix Code with following Information (space separated Values):
  - Order Code
  - MAC Address QCA7005
  - MAC Address Host
  - Serial Number

8 Order Code Compilation

Product Family Code	SW stack Variant	Plug type	61851 Interface Type	Customer Interface	HW version	SW Version	customize variant	packaging
I2CME-	**D: Dual (ISO and DIN)**	**M: Type 2**	**N: Native GPIO**	**C: CAN**	**-01 (C-Sample)**	**-00 (dev)**	**-00 (none)**	-T: Tray
	P: ISO 15118 PnC*	**J: Type 1**	**B: By customer**	S: SPI*				-R: Reel
	V: ISO 15118 V2G*			E: Ethernet*				

*under development

9 Order Information

The following table provides an overview of the available Charge Module E variants

Order Code	SW Stack	Plug Type	IEC 61851 Interface	Customer Interface	Packaging	Availability
I2CME-DMBC-01-00-00-T	Dual	Type 2	by Customer	CAN	Tray	standard
Order Code	SW Stack	Plug Type	IEC 61851 Interface	Customer Interface	Packaging	Availability
I2CME-DMNC-01-00-00-T	Dual	Type 2	Native GPIO	CAN	Tray	standard

10 Handling

This electronic component is sensitive to electrostatic discharge (ESD).

- Process the modules according to IPC/JEDEC J–STD-020 and J-STD-033 guidelines.
- Limit repeated reflow processes to maximum 2.

Detailed information will be added later.

11 Revisions

Revision	Release Date	Changes
6	19 September 2022	Add Module Dimensions Added UART Pins Updated figure "Module Dimensions" Updated company contact Updated the key features and module interfaces Removed PP schematics
5	16 November 2021	Updated Figure 4 (EVSE CP generation and voltage read reference schematic) Updated table Module Pinout Updated table Supply parameter (changed min. DC supply voltage to 3.13V)
4	19 October 2021	Corporate Identity Beautified Figures
3	18 October 2021	Updated CP generation reference schematic
2	17 June 2021	Added Schematics UDS protocol feature Added Zero cross detection Added Pin 1 marking at mechanical dimensions Updated Module marking
1	18 May 2021	Initial release

12 Contact

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