PLC Stamp Multi VERT Datasheet

chargebyte GmbH

Nov 13, 2023

Contents

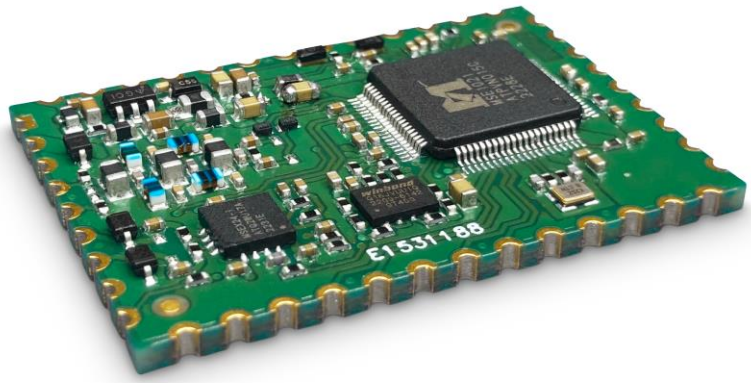

Figure 1 PLC Stamp Multi VERT

1 Revisions

Revision	Release Date	Changes
1	November 13th 2023	initial release

2 Introduction

The PLC Stamp Multi is a versatile PowerLine Communication (PLC) module that can be interfaced with the host through either a traditional SPI interface or a 100BaseT Ethernet port. The VERT version of the PLC Stamp Multi features Vertexcom's MSE1021 chipset. Specifically designed for electric vehicle charging systems, it complies with the ISO 15118 standard, suitable for the Combined Charging System (CCS).

3 Key Features

- ISO 15118-3 compliant
- low power consumption
- small footprint
- SPI and 100BaseT Ethernet interface

4 Operational

Parameter	Value
Outline dimension	35.56 mm × 25.40 mm x 3.15 mm
Power supply	+5.0 V and +3.3 V
Current consumption	max. 150mA on 5 V, max 200 mA on 3.3 V
Temperature range	-40 °C to +85 °C
Weight	5 g
RoHS / REACH	This product is manufactured RoHS / REACH compliant.

Table 1 Operational Parameters

5 Module Overview

This block diagram shows the module components in the gray box as well as the connections and external components that are needed additionally.

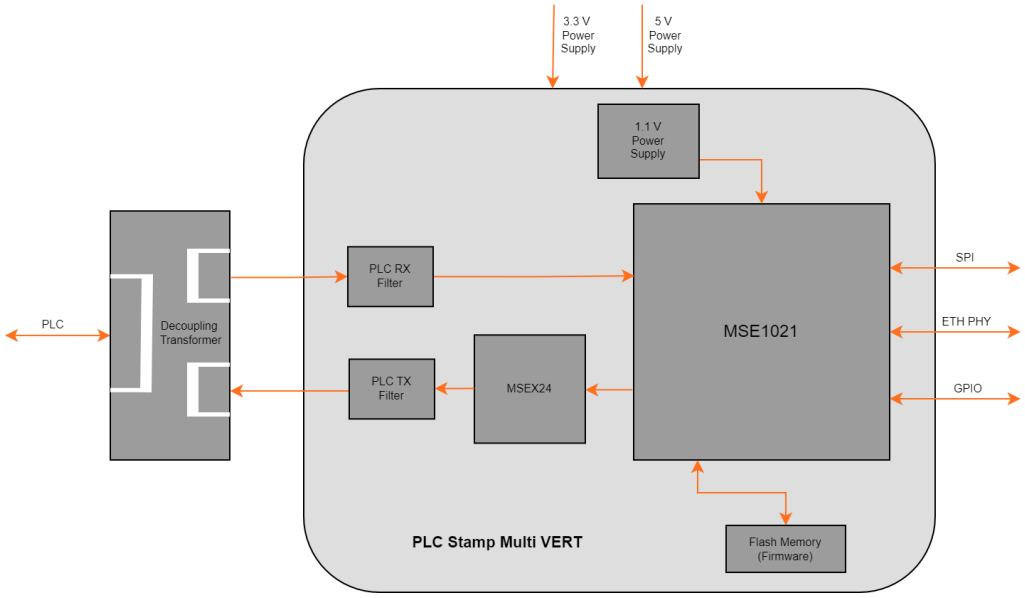

Figure 2 Block Diagram of PLC Stamp Multi VERT

6 Electrical Characteristics

6.1 Absolute maximum ratings

Stresses beyond these limits will cause permanent damage to the device.

Maximum parameter	Min	Max	Unit
+3.3 V supply voltage	-0.30	+3.63	V
+5.0 V supply voltage	-0.30	+5.50	V

Table 2 Absolute Maximum Ratings

6.2 Recommended operating conditions

Supply Parameter	Min	Typ	Max	Unit
+3.3 V supply voltage	+3.13	+3.30	+3.47	V
+5.0 V supply voltage	+4.75	+5.00	+5.25	V

Table 3 Recommended operating conditions

7 Thermal Characteristics

Maximum parameter	Min	Max	Unit
Ambient Operating Temperature	-40	+85	°C
Storage Temperature	-40	+95	°C
Relative air humidity (not condensing)	10	90	%

Table 4 Thermal Characteristics

8 Module Pinout

Pin	Name	Direction	Functional Description
1	GND	SUPPLY	Ground connection
2	+3V3	SUPPLY	3.3 V supply voltage to the module
3	GND	SUPPLY	Ground connection
4	CPL_RX_P	INPUT	Powerline receiver differential positive input
5	CPL_RX_N	INPUT	Powerline receiver differential negative input
6	CPL_TX_P	OUTPUT	Powerline transmitter differential positive output
7	CPL_TX_N	OUTPUT	Powerline transmitter differential negative output
8	GND	SUPPLY	Ground connection
9	RSVD_01	NC	Reserved for future use, no connection
10	GND	SUPPLY	Ground connection
11	RSVD_02	NC	Reserved for future use, no connection
12	RSVD_03	NC	Reserved for future use, no connection
13	EPHY_RX_N	INPUT	100Base-T Ethernet PHY reciever differential negative input
14	EPHY_RX_P	INPUT	100Base-T Ethernet PHY reciever differential positive input
15	GND	SUPPLY	Ground connection
16	EPHY_TX_N	OUTPUT	100Base-T Ethernet PHY transmitter differential negative output
17	EPHY_TX_P	OUTPUT	100Base-T Ethernet PHY transmitter differential positive output
18	EPHY_LED0	OUTPUT	Ethernet Jack LED, linked status indicator
19	EPHY_LED1	OUTPUT	Ethernet Jack LED, activity indicator
20	RSVD_04	NC	Reserved for future use, no connection
21	RSVD_05	NC	Reserved for future use, no connection
22	RSVD_06	NC	Reserved for future use, no connection
23	GND	SUPPLY	Ground connection
24	RSVD_07	NC	Reserved for future use, no connection
25	RSVD_08	NC	Reserved for future use, no connection
26	RSVD_09	NC	Reserved for future use, no connection
27	RSVD_10	NC	Reserved for future use, no connection
28	MFIO_01	IN / OUT	Configurable MFIO / Hardware bootstrap setting SPI Mode
29	MFIO_02	IN / OUT	Configurable MFIO
30	RSVD_11	NC	Reserved for use on other chipset variants of the PLC Stamp Multi, no connection
31	HSL_DATA3	INPUT	Hardware Bootstrap setting Host Mode
32	GND	SUPPLY	Ground connection
33	RSVD_12	NC	Reserved for future use, no connection
34	MFIO_03	IN / OUT	Hardware bootstrap setting ETH Mode
35	SPI_S_CS	INPUT	SPI interface Chip Select signal (input when MSE1021 is set to SPI slave mode) (low active)
36	SPI_S_MOSI	INPUT	SPI interface MOSI signal (input when MSE1021 is set to SPI slave mode) / Hardware bootstrap setting ETH Mode
37	SPI_S_CLK	INPUT	SPI interface Clock signal (input when MSE1021 is set to SPI slave mode) / Hardware bootstrap setting ETH Mode
38	SPI_S_INT	OUTPUT	SPI interface Interrupt signal (output when MSE1021 is set to SPI slave mode) / Hardware bootstrap setting MAC Mode
39	SPI_S_MISO	OUTPUT	SPI interface MISO signal (output when MSE1021 is set to SPI slave mode)
40	MCU_RESET	INPUT	MSE1021 reset signal (low active)
41	GND	SUPPLY	Ground connection
42	GND	SUPPLY	Ground connection
43	GND	SUPPLY	Ground connection
44	+5 V	SUPPLY	5 V supply voltage to the module

Table 5 Module Pinout

9 Hardware Bootstrap Configuration

There are 6 pins which are used as Hardware Bootstraps, setting the configuration the MSE1021 on the PLC Stamp Multi VERT module will boot.

These Pins are being treated as INPUTs during the bootup phase and their state will be read, before they will be switched to their actual function listed above.

All Hardware Bootstraps require a 10 kOhm resistor to either +3.3 V or GND, depending on the desired configuration:

9.1 Host Mode

This option will set the interface with which the MSE1021 can be communicated with.

HSL_DATA3	MSE1021 Host Mode
Pull Down	SPI interface will be used. Settings concerning the Ethernet interface will be ignored.
Pull Up	Ethernet interface will be used. Settings concerning the SPI interface will be ignored.

Table 6 Host Mode configuration

9.2 SPI Mode (for SPI interface only)

If the device is set to SPI interface mode, this option will set whether the SPI will operate in Master or Slave mode.
The default communication mode is SPI Slave.
The MSE1021 requires a SPI clock speed of 6 to 7 MHz and
SPI Mode 3 (CPOL = 1, CPHA = 1).

MFIO_01	MSE1021 SPI Mode
Pull Down	SPI Master
Pull Up	SPI Slave

Table 7 SPI Mode configuration

9.3 Ethernet Mode (for Ethernet interface only)

These Hardware Bootstraps will choose the type of Ethernet interface the module will boot up in. Ethernet PHY mode is currently supported; all other combinations are reserved for future use or illegal.

SPI_S_MOSI	MFIO_03	SPI_S_CLK	MSE1021 ETHERNET MODE
Pull Down	Pull Down	Pull Down	EPHY

Table 8 Ethernet Mode configuration

9.4 MAC Mode

If the device is set to Ethernet PHY mode pulling this pin low will enable the 100Base-T port. The other option is reserved for future use.

SPI_S_INT	MSE1021 MAC Mode
Pull Down	Enable 100Base-T port

Table 9 MAC Mode configuration

10 Module Dimensions

This figure shows the physical dimensions of the module. Pin 1 is a rectangular shaped pad on the top side of the module.

All dimensions are in mm, the pads are all of the same size and distances between pads are equal if not otherwise specified in the drawing.

The board outline dimensions have a tolerance of ±0.2mm.

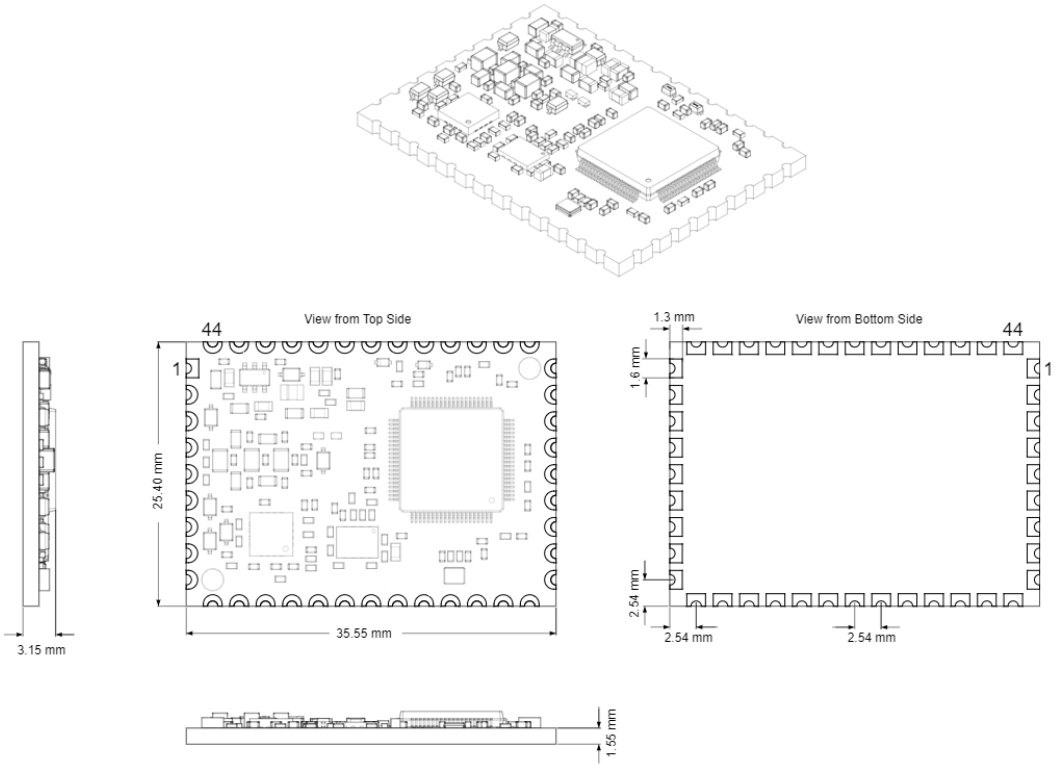

Figure 3 Module Dimensions

11 Footprint Dimensions

This figure shows the recommended footprint for the PLC Stamp Multi VERT. The module outline shows the ideal measures, tolerance is not included.

The restricted area should not be used for signal routing and must be fully covered with soldermask.

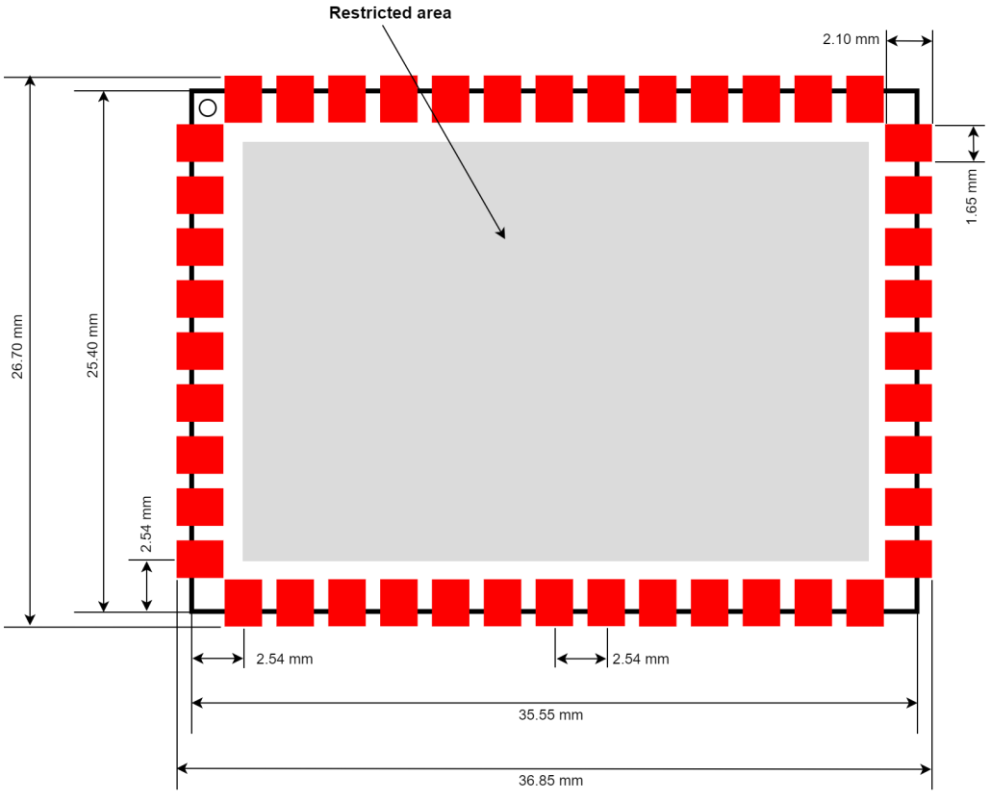

Figure 4 Footprint Dimensions

12 Reference Schematic

This reference is loosely based on the Vertexcom's MSE1021 chipset datasheet and provides guidance in the default implementation of the PLC Stamp Multi VERT.

All necessary non-standard parts can be purchased through chargebyte GmbH.

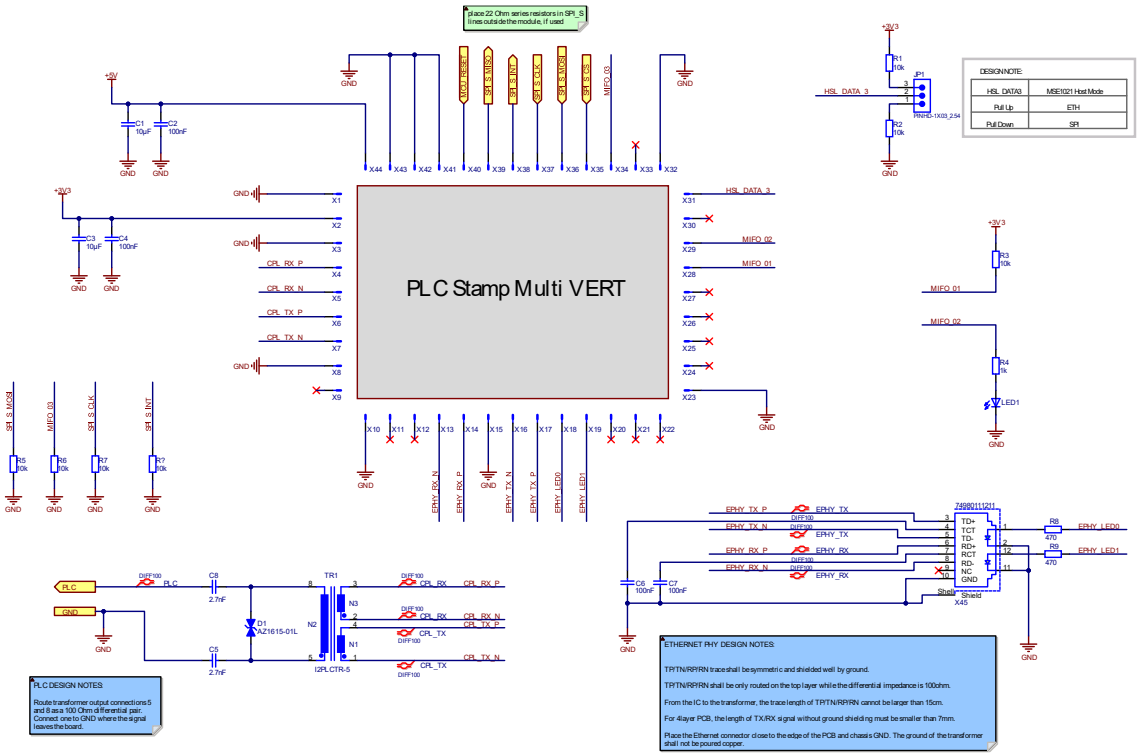

Figure 5 PLC Stamp Multi VERT Reference Schematic

13 Module Marking

Detailed information will be added later.

14 Order Information

Product Family Code	Chip	Serial Interface	Parameter Optimization	Version	Packaging
I2STML-	V: (Vertexcom)	SE: (SPI, EPHY)	E: Automotive EVSE	000: (B - Sample)	-T: Tray
					-R: Reel

Table 10 PLC Stamp Multi Family Code Compilation

Order Code	Temperature Range/ °C	Serial Interface	Parameter Optimization	Packaging	Availability	Comment
I2STML-VSEE-000	-40 to +85	SPI, EPHY	Automotive EVSE		standard	B-Sample

Table 11 PLC Stamp Multi VERT Order Code

15 Handling

This electronic component is sensitive to electrostatic discharge (ESD).

- Process the modules according to IPC/JEDEC J–STD-020 and J-STD-033 guidelines.
- Limit repeated reflow processes to maximum 2.

16 Packaging

Detailed information will be added later.

17 Contact

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